8

TIMEKEEPING CIRCUITS

CMOS TIMEKEEPING CIRCUITS

Type	Description	Display Type	Voltage Range	Page No.
5201	3 1/2 Digit Hours/Minutes/Seconds Decoder – Driver	D.S. LCD	10-15	8-3
5201-2	3 1/2 Digit Hours/Minutes/Seconds Decoder – Driver	F.E. LCD	6-10	8-3
5202	3 1/2 Digit Hours and Minutes Decoder – Driver	D.S. LCD	10-15	8-3
5202-2	3 1/2 Digit Hours and Minutes Decoder – Dfiver	F.E. LCD	6-10	8-3
5204	3 1/2 Digit Time/Seconds/Date Decoder – Driver	F.E. LCD	6-10	8-7
5801	32.768 kHz Oscillator – Divider	N.A.	1.2-1.6	8-11

LIQUID CRYSTAL DISPLAY DECODER-DRIVER

- **5201 and 5202 Drive Dynamic Scattering Displays**
- **5201-2 and 5202-2 Drive Field Effect Displays**
- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **5201 and 5201-2 Display Hours, Minutes and Seconds on Command**
- **5202 and 5202-2 Display Hours and Minutes**
- **Inputs Protected Against Static Discharge**

The 5201, 5201-2, 5202, and 5202-2 are low power 3½ digit liquid crystal display decoder/drivers intended for use in electronic timekeeping applications such as wristwatches and battery-operated clocks. The 5201 and 5202 are specified for operation over the supply voltage range 10 to 15 volts for use with dynamic scattering liquid crystal displays. The 5201-2 and 5202-2 are specified for operation from 6 to 10 volt supply voltages for use with field effect liquid crystal displays.

The 5201 and 5201-2 normally display hours and minutes. On activation of the seconds command switch, seconds are displayed in the minutes position and hours are blanked. Resetting of the seconds command switch restores the display mode to hours and minutes. The 5202 and 5202-2 display hours and minutes only. The colon is flashed at a 1 Hz rate on all four devices.

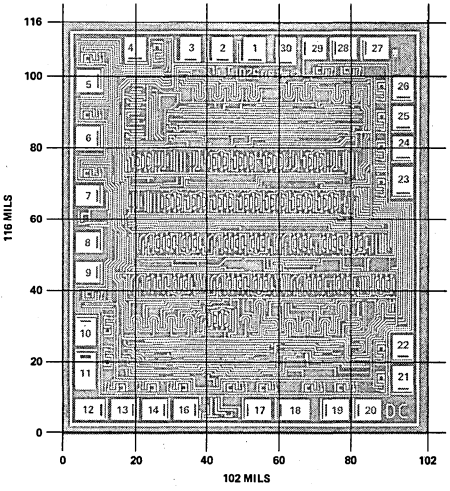
These decoder/drivers accept a 64 Hz input signal from which they count and decode hours and minutes (and seconds in the case of the 5201 and 5201-2). The decoded signals are used for driving the three 7-segment and one 2-segment display digits. A symmetrical 32 Hz signal is provided to drive the common back plate of the display. Segments to be energized are driven with a symmetrical 32 Hz signal that is out-of-phase with the common signal while unenergized segments are driven with a symmetrical 32 Hz signal in phase with the common signal.

Two inputs allow for time setting and resetting. (See page 8-5 for description of operation.)

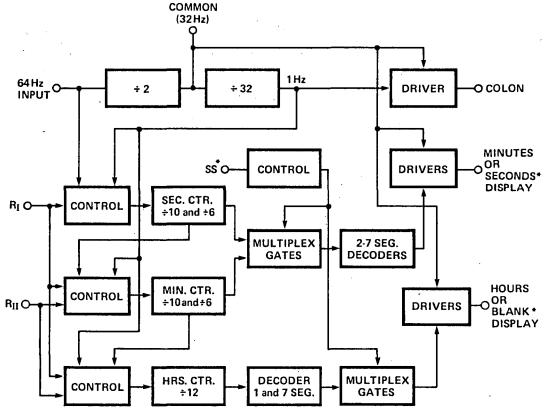
These devices are fabricated with complementary MOS silicon gate technology. This extremely low power technology is ideally suited for the manufacture of devices designed to operate from small batteries for long periods of time.

CHIP TOPOGRAPHY

(Numbers refer to package pin number.)



BLOCK DIAGRAM



(*5201 AND 5201-2 ONLY)

Absolute Maximum Ratings*

Temperature Under Bias ..... −20°C to +70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage V_{DD} with respect to GND ..... −0.3V to +18.0V
Voltage on all Inputs or Outputs with respect to GND ..... −0.3V to V_{DD} +0.3V
Power Dissipation 100mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics for 5201 and 5202

Dynamic Scattering Liquid Crystal Display Applications (T_A = 25°C; 10V ≤ V_{DD} ≤ 15V; f_{IN} = 64Hz unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}(Avg.)	Average Operating Current			500	nA	V_{DD} = 15V; t_{pwc} = 25μs; t_f = 0.5μs; t_r = 35μs; outputs open
I_{DD}(Static)	Static Current			300	nA	V_{DD} = 15V; 64Hz input open; outputs open
I_{IL}	Input Low Current	−5	−13	−28	μA	V_{DD} = 15V; V_{IN} = 1.2V
V_{IL}	Input Low Voltage	−0.3		1.2	V	V_{DD} = 15V
V_{IH}	Input High Voltage	14.0		15.3	V	V_{DD} = 15V
V_{OLC}	Output Low Voltage Common			0.1 0.1	V V	V_{DD} = 15V; I_{OLC} = 1.5μA V_{DD} = 10V; I_{OLC} = 1.0μA
V_{OHC}	Output High Voltage Common	14.9 9.9			V V	V_{DD} = 15V; I_{OHC} = −1.5μA V_{DD} = 10V; I_{OHC} = −1.0μA
V_{OLS}	Output Low Voltage Segments			0.1 0.1	V V	V_{DD} = 15V; I_{OLS} = 0.1μA V_{DD} = 10V; I_{OLS} = 0.06μA
V_{OHS}	Output High Voltage Segments	14.9 9.9			V V	V_{DD} = 15V; I_{OHS} = −0.1μA V_{DD} = 10V; I_{OHS} = −0.06μA

D.C. and Operating Characteristics for 5201-2 and 5202-2

Field Effect Display Applications (T_A = 25°C; 6V ≤ V_{DD} ≤ 10V; f_{IN} = 64Hz unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD} (Avg.)	Average Operating Current			600	nA	V_{DD} = 10V; t_{pwc} = 25μs; t_f = 0.5μs; t_r = 75μs; outputs open
I_{DD} (Static)	Static Current			400	nA	V_{DD} = 10V; 64Hz input open; outputs open
I_{IL}	Input Low Current	−0.5	−1.5		μA	V_{DD} = 6.0V; V_{IN} = 1.2V
V_{IL}	Input Low Voltage	−0.3		1.2	V	V_{DD} = 10V
V_{IH}	Input High Voltage	9.0		10.3	V	V_{DD} = 10V
V_{OLC}	Output Low Voltage Common			25 50	mV mV	V_{DD} = 10V; I_{OLC} = 0.15μA V_{DD} = 6V; I_{OLC} = 0.1μA
V_{OHC}	Output High Voltage Common	9.975 5.950			V V	V_{DD} = 10V; I_{OHC} = −0.15μA V_{DD} = 6V; I_{OHC} = −0.1μA
V_{OLS}	Output Low Voltage Segments			25 50	mV mV	V_{DD} = 10V; I_{OLS} = 10nA V_{DD} = 6V; I_{OLS} = 6nA
V_{OHS}	Output High Voltage Segments	9.975 5.950			V V	V_{DD} = 10V; I_{OHS} = −10nA V_{DD} = 6V; I_{OHS} = −6nA

A.C. Characteristics for 5201 and 5202 ($T_A = 25°C$; $f_{in} = 64Hz$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	Input Pulse Width	10	15	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time			0.5	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$
t_r	Input Pulse Rise Time			35	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$

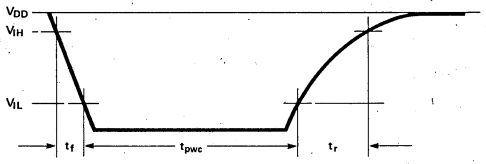
A.C. Characteristics for 5201-2 and 5202-2 ($T_A = 25°C$; $f_{in} = 64Hz$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	Input Pulse Width	10	15	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time			0.5	μs	$V_{IL} = 1.2V$; $V_{IH} = 14V$; $V_{DD} = 15V$
t_r	Input Pulse Rise Time			75	μs	$V_{IL} = 1.2V$; $V_{IH} = 9V$; $V_{DD} = 10V$

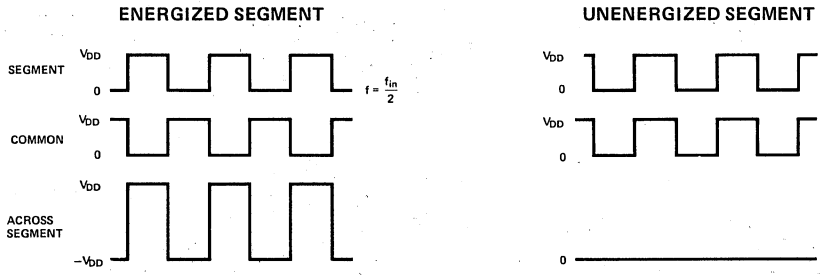
Capacitance ($T_A = 25°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		2.8	5	pF	Capacitances are measured in 30 lead flatpack with all pins except the test pin at ground, f = 1MHz.
C_{OUTC}	Output Capacitance Common		8.5	15	pF	
C_{OUTS}	Output Capacitance Segments		2.0	5	pF	

Input Waveform



Output Waveforms

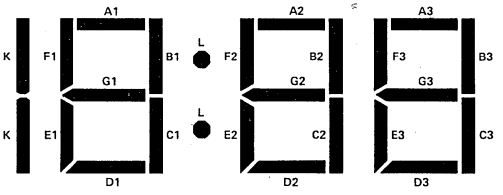


Time Setting

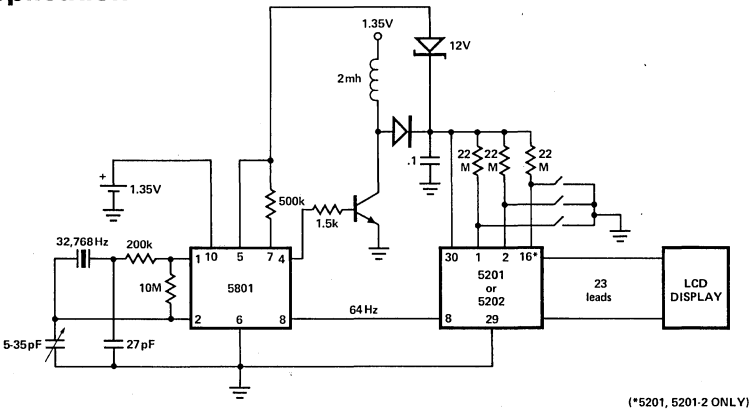
Two inputs (Reset I and Reset II) allow setting and synchronization of the time to a time standard. The operation of these two inputs is described by the following table:

State	Reset I	Reset II	Operation
B_1	V_{DD}	V_{DD}	Normal
B_2	V_{DD}	0	Clock Running, hours are advanced at 1Hz
B_3	0	0	Seconds counter is reset to 00 sec.; minutes are advanced at 1Hz rate; hours are incremented by 1 if minutes exceed 59, otherwise they are unaffected.
B_4	0	V_{DD}	Seconds counter reset to 00 sec.; minutes are held if state B_4 is entered directly from state B_3; hours are unaffected. Note: Minutes will be incremented by one if state B_4 is entered from state B_1 or B_2.

Display Segment Format

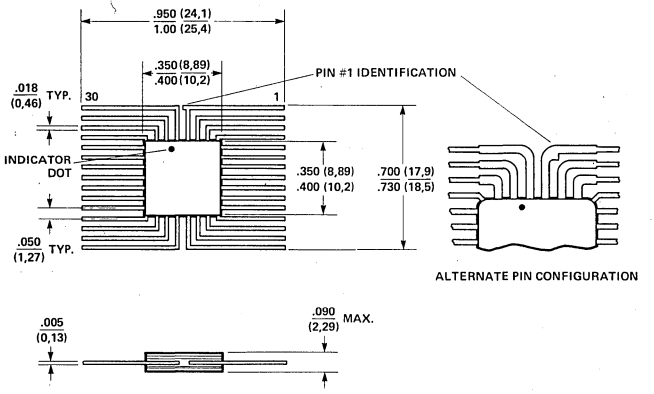


Typical Application



(*5201, 5201-2 ONLY)

Packaging Information



PIN ASSIGNMENT

Pin No.	Function	Pin No.	Function
1	Reset II	16	Seconds Switch*
2	Reset I	17	B3
3	Common	18	A3
4	K	19	F3
5	E1	20	G3
6	D1	21	B2
7	C1	22	A2 + D2
8	64Hz In	23	F2
9	L (Colon)	24	G2
10	E2	25	B1
11	C2	26	A1
12	E3	27	F1
13	D3	28	G1
14	C3	29	Ground
15	N/C	30	V_{DD}

*5201 and 5201-2 only

TIME/SECONDS/DATE LIQUID CRYSTAL DISPLAY DECODER-DRIVER

- **Displays Hours and Minutes or Seconds or Date**
- **Pin Compatible with Intel 5201 and 5202**
- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **Anti-Bounce Circuitry on Switch Inputs**
- **Drives 3½ Digit Field Effect Displays**
- **Inputs Protected Against Static Discharge**

The 5204 is a low power 3-½ digit liquid crystal display decoder driver intended for use in 12 hour timekeeping applications such as wristwatches and battery-operated clocks.

The 5204 accepts a 64 Hz input signal from which it counts and decodes Seconds, Minutes, Hours, and Date. The decoded signals are used for driving the three 7-segment and one 2-segment display digits. A symmetrical 32 Hz signal is provided to drive the common back plate of the display. Segments to be energized are driven with a symmetrical 32 Hz signal that is out-of-phase with the common signal while unenergized segments are driven with a 32 Hz signal in phase with the common signal.

The 5204 will normally display Hours and Minutes. Depression of the D/C command switch will cause Seconds to be displayed in the Minutes position and the Hours will be blanked. A second depression of the D/C command switch will cause the Date to be displayed in the Minutes position and the Hours to be blanked. A third depression of the D/C command switch will cause a return to normal mode displaying Hours and Minutes. The colon is flashed at a 1 Hz rate in all three display modes.

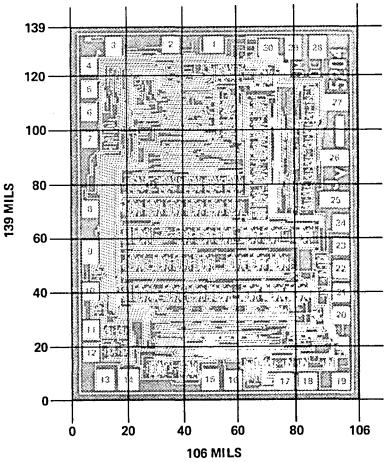
A separate switch is used for timesetting. Thus only two switches are required for operation of the watch. (See page 8-9 for description of operation.)

The 5204 is designed to operate in conjunction with the 5801 oscillator-divider circuit. For information on the 5801 see the 5801 data sheet.

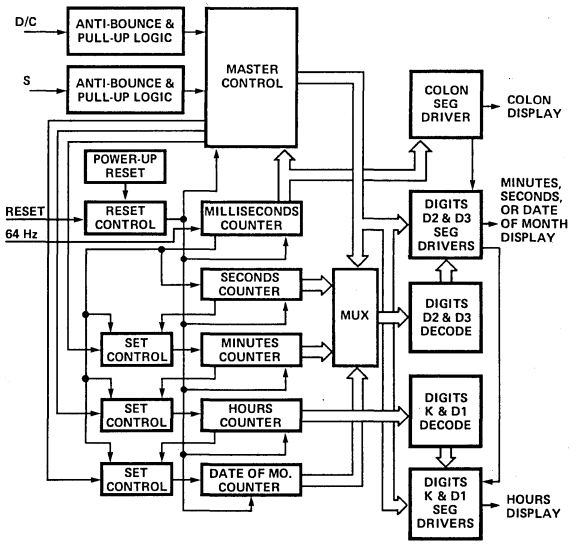
This device is fabricated with complementary MOS silicon gate technology. This extremely low power technology is ideally suited for the manufacture of devices designed to operate from small batteries for long periods of time.

CHIP TOPOGRAPHY

(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... −20°C to +70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage V_{DD} with respect to GND ..... −0.3V to +18.0V
Voltage on all Inputs or Outputs with respect to GND ..... −0.3V to V_{DD} +0.3V
Power Dissipation 100mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 25°C$; $6V \leq V_{DD} \leq 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
I_{DD}	Total Average Internal Current		500	nA	$V_{DD} = 10V$; $t_{pwc} = 25\mu s$; $t_f = 0.5\mu s$; $t_r = 75\mu s$; Outputs Open
I_{ILC}	64 Hz Input Low Current (Clock)	2.0	-15	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$
I_{ILS}	Switch Input Low Current (D/C, S)	-1.0	-50	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$ 64 Hz Input Voltage = 0.0V Note 1
V_{IL}	Input Low Voltage	-0.3	1.2	V	
V_{OLC}	Output Low Voltage Common		25	mV	$V_{DD} = 10V$; $I_{OLC} = 1.0\mu A$
V_{OHC}	Output High Voltage Common	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHC} = -1.0\mu A$
V_{OLS}	Output Low Voltage Segment		25	mV	$V_{DD} = 10V$; $I_{OLS} = 0.1\mu A$
V_{OHS}	Output High Voltage Segment	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHS} = -0.1\mu A$
I_{ILR}	Reset Input Low Current	-1.0	-200	μA	$V_{DD} = 10V$

A.C. Characteristics

$T_A = 25°C$; $6V \leq V_{DD} \leq 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

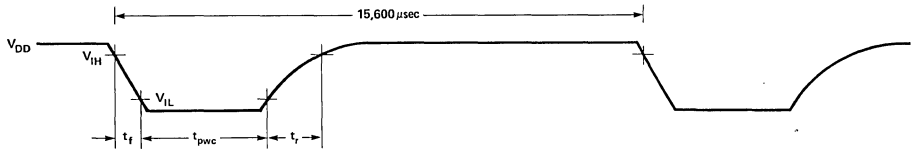
Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{pwc}	Input Pulse Width (Clock)	10	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time		0.5	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_r	Input Pulse Rise Time		75	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_{sd}	Switch Delay	32	80	ms	Note 2

Capacitance ($T_A = 25°C$)

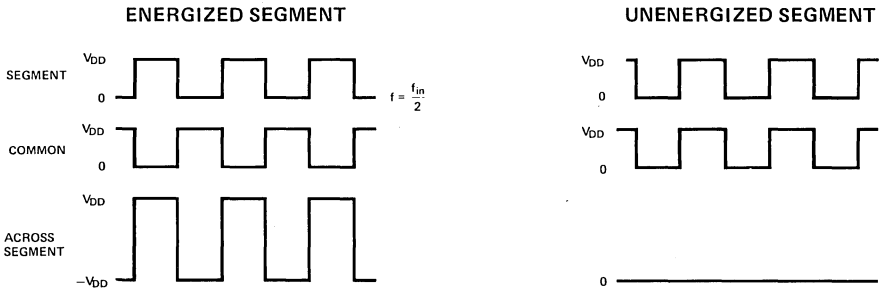
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		2.8	5	pF	Capacitances are measured in 30 lead flatpack with all pins except the test pin at ground, f = 1MHz.
C_{OUTC}	Output Capacitance Common		8.5	15	pF	
C_{OUTS}	Output Capacitance Segments		2.0	5	pF	

NOTES: 1. All switch inputs include dynamic pull-up circuitry which is clocked in synchronization with the 64 Hz input. The average current drawn by these inputs in the low state will be proportional to the duty cycle of the 64 Hz input. The value specified is for the case where the 64 Hz input is held low. (100% duty cycle).
2. The D/C and S switch inputs include anti-bounce circuitry. This circuitry requires that a switch input be stable for 2 consecutive 32 Hz clock periods in order to be recognized as a valid input. Switch delay is the time during which the antibounce circuitry is determining a valid, stable input.

Input Waveform

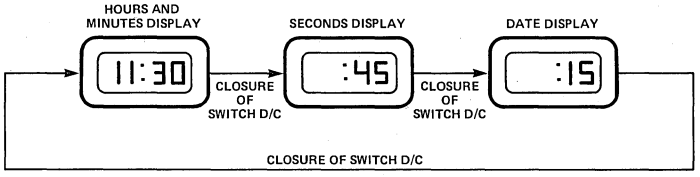


Output Waveforms



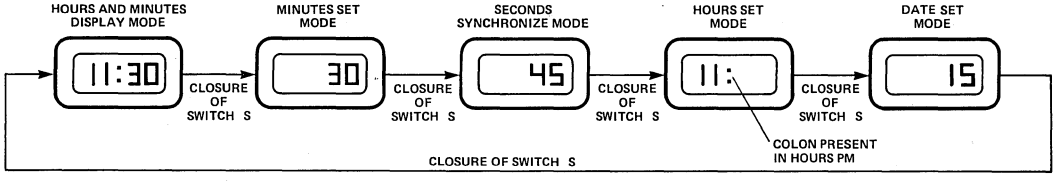
Time Display

Switch input D/C controls the time display modes. Each closure of switch D/C (D/C input = low) causes a change in the display mode in the sequence Hours and Minutes→Seconds→Date→Hours and Minutes. The following diagram illustrates this:



Time Setting

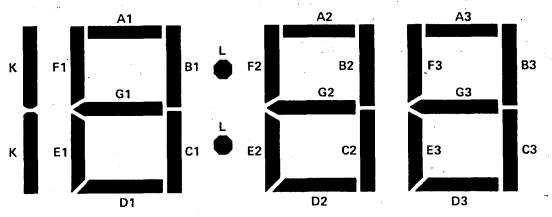
Switch input S controls the time setting modes. This switch input is active only when the circuit is in the Hours and Minutes display mode. Each closure of switch S (S input = low) causes a change in the time set modes in the sequence Hours and Minutes→Minutes→Seconds →Hours→Date→Hours and Minutes. *Closure of switch D/C when in the Minutes, Hours, or Date time set modes will cause that mode to be advanced at a 1 Hz rate. Closure of switch D/C in the Seconds synchronize mode will cause the Minutes to be advanced by one and the Seconds to be reset to zero and held until the D/C input is returned high.* The colon is displayed only in the Hours PM state in the time set mode. The following diagram illustrates this:



Reset

The reset input may be used to initialize all time counters to the zero state. All time counters are automatically reset to zero when voltage is initially applied to the circuit. The zero state is 12:00 AM, 00 Seconds, 0 Date.

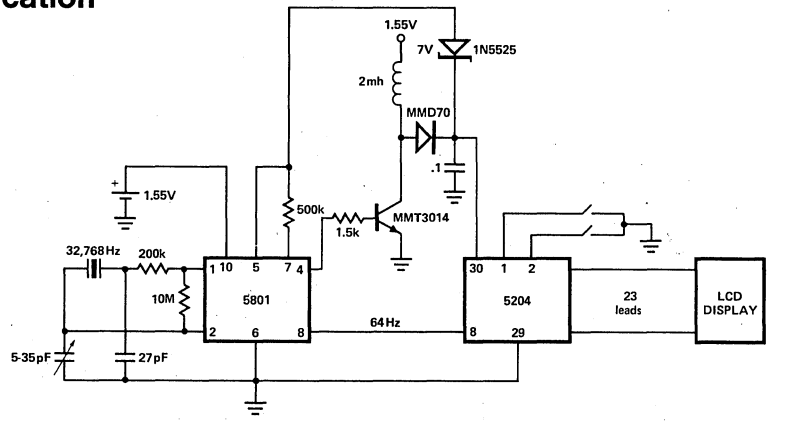
Display Segment Format



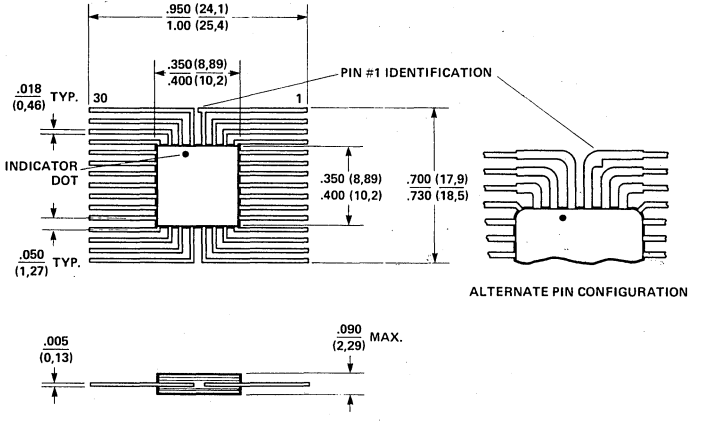
DIGITS D1, D2 AND D3 TRUTH TABLE

NUMBER	SEGMENTS						
	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Typical Application



Packaging Information



PIN ASSIGNMENT

Pin No.	Function	Pin No.	Function
1	D/C	16	N/C
2	S	17	B3
3	Common	18	A3
4	K	19	F3
5	E1	20	G3
6	D1	21	B2
7	C1	22	A2 + D2
8	64Hz In	23	F2
9	L (Colon)	24	G2
10	E2	25	B1
11	C2	26	A1
12	E3	27	F1
13	D3	28	G1
14	C3	29	Ground
15	Reset	30	V_{DD}

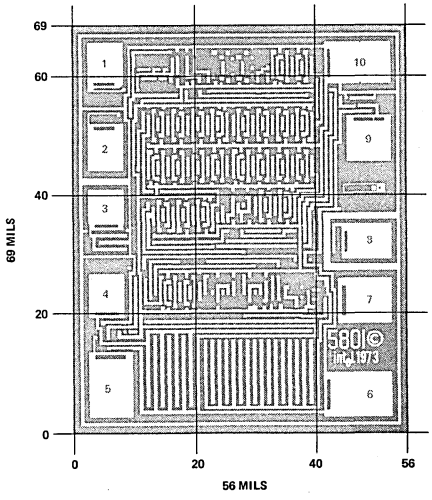
LOW POWER OSCILLATOR-DIVIDER

- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **On Chip Drive and Regulator Circuitry for Up-Converter**
- **Long Battery Life--Low Current Drain--5 μA max.**
- **Inputs Protected Against Static Discharge**

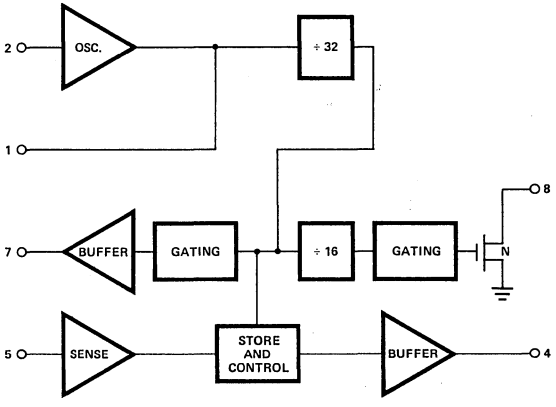
The 5801 is a low power oscillator and 2^9 divider ideally suited for use in battery powered timekeeping applications. The circuitry consists of an inverter stage designed to operate in conjunction with an external quartz crystal and feedback network to form an oscillator, a 9-stage binary ripple carry counter, and control logic. Two outputs are provided: A buffered drive output providing ½ cycle of the oscillator at a repetition rate equal to the frequency of the oscillator divided by 2^5 and an open drain output that is switched on for ½ cycle of the oscillator at a repetition rate of the oscillator divided by 2^9. The buffered drive output and associated control circuitry are designed for use with external components to implement a regulated voltage up-converter.

The 5801 is manufactured with complementary MOS silicon gate technology. Long term continuous operation from small batteries is made possible by use of this low power technology.

CHIP TOPOGRAPHY
(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−20°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage (V_{DD})	−0.3V to +8.0V
Voltage on Output (pin 8) with respect to V_{SS}	−0.3V to +18.0V
Voltage on all other pins	−0.3V to V_{DD} +0.3V
Power Dissipation	80mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics (T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{DD}	Average Supply Current		3.0	5.0	μA	V_{DD} = 1.4V, Note 1
V_{DDS}	Oscillation Start Voltage	1.2			V	Note 1
I_{OLC}	64Hz N-Channel Open Drain Output Current	50			μA	V_{DD} = 1.2V; V_{OLC} = 1.2V
I_{OHD}	1024Hz Drive P-Channel Output Current	−500			μA	V_{DD} = 1.2V; V_{OHD} = 0.7V
I_{OLD}	1024Hz Drive N-Channel Output Current	200			μA	V_{DD} = 1.2V; V_{OLD} = 0.5V
I_{OLS}	1024Hz Sample N-Channel Output Current	10			μA	V_{DD} = 1.2V; V_{OLS} = 0.15V
V_{IL}	Sense Low Input Voltage			0.4	V	V_{DD} = 1.2V
V_{IH}	Sense High Input Voltage	0.9			V	V_{DD} = 1.2V
V_{BDC}	64Hz N-Channel Breakdown Voltage	15.0			V	V_{DD} = 1.2V; I_{BDC} = 1.0μA

Note 1. Frequency of oscillation = 32,768Hz when connected as shown in Figure 1.

Test Circuit

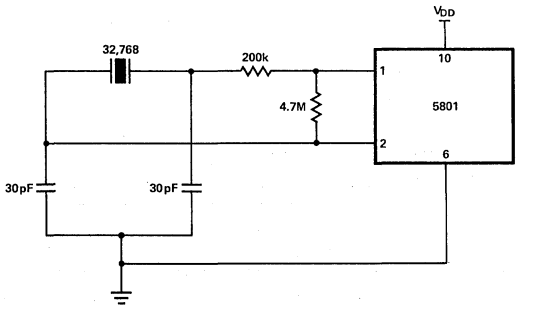


Figure 1.

A.C. Characteristics $T_A = 25°C$

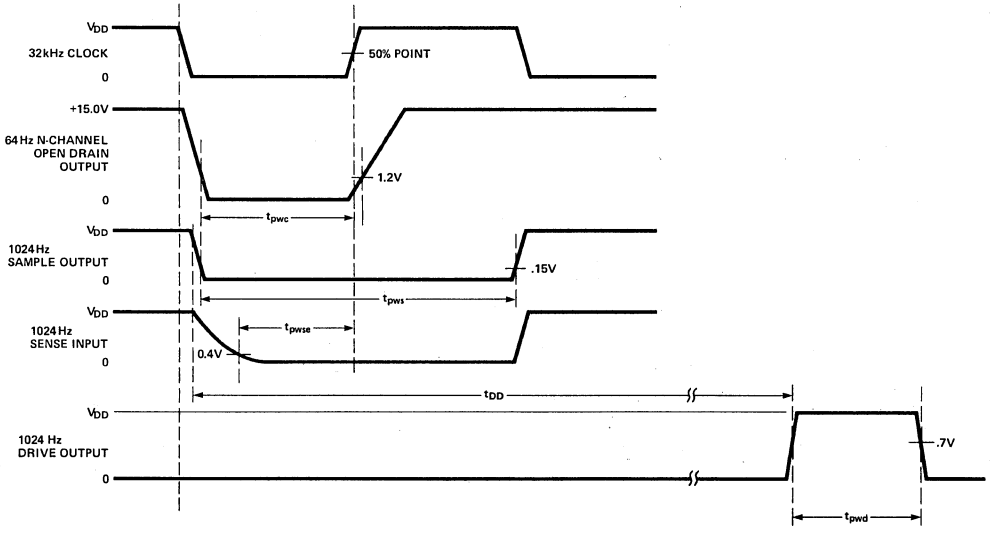
Symbol		Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	64Hz N-Channel Open Drain Output Pulse Width	10		25	μs	V_{DD} = 1.2V, 1.4V; 64Hz
t_{pws}	1024Hz Sample Output Pulse Width	25		35	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{pwd}	1024Hz Drive Output Pulse Width	13		17	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{dd}	1024Hz Sample Output to Drive Output Delay	485		520	μs	V_{DD} = 1.2V, 1.4V; 1024Hz
t_{pwse}	1024Hz Sense Input Pulse Width	5			μs	V_{DD} = 1.2V, 1.4V; 1024Hz

Capacitance

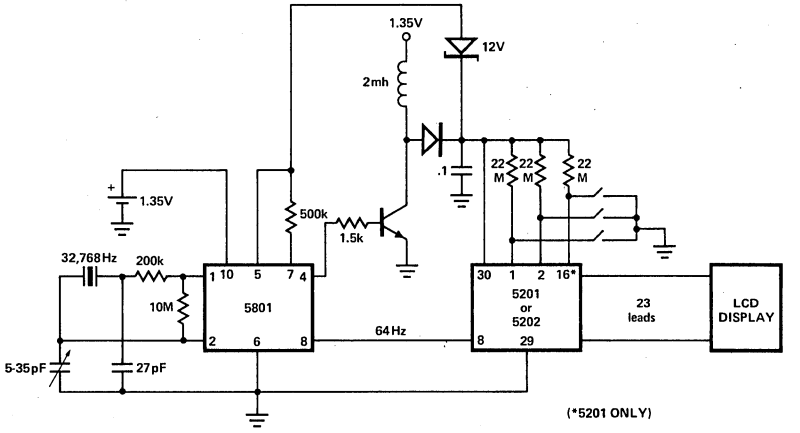
Symbol	Test	Typ.	Max.	Unit
C_{IN2}	Input Capacitance at pin 2 V_{IN} = 0V	3.2	8.0	pF
C_{IN5}	Input Capacitance at pin 5 V_{IN} = 0V	2.2	6.0	pF
C_{OUT1}	Output Capacitance at pin 1 V_{OUT} = 0V	3.0	8.0	pF
C_{OUT4}	Output Capacitance at pin 4 V_{OUT} = 0V	23	35	pF
$C_{OUT\ 7,8}$	Output Capacitance at pins 7,8; V_{OUT} = 0V	2.4	6.0	pF

Note: All capacitance values are measured in 10 lead flatpack with pins 6, 10 and all other untested pins tied to ground.

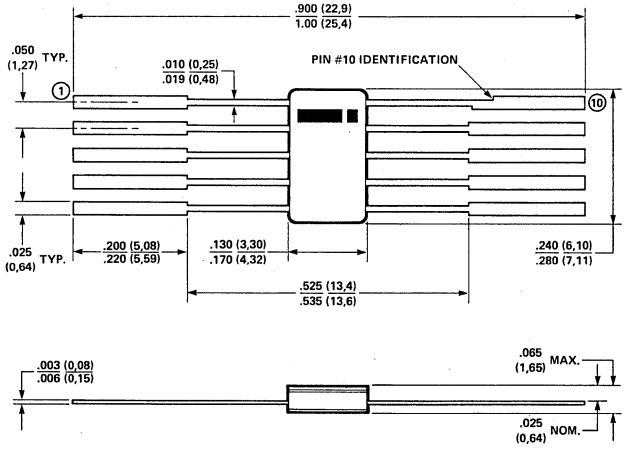
Timing Diagram



Typical Application



Packaging Information



PIN ASSIGNMENT

Pin #	Function
1	OSC INV OUT
2	OSC INV IN
3	N/C
4	1024Hz OUT (Drive)
5	1024Hz IN (Sense)
6	GROUND
7	1024Hz OUT (Sample)
8	64Hz OUT (N-CH)
9	N/C
10	V_{DD}

SINGLE CHIP LCD TIME/SECONDS/DATE WATCH CIRCUIT

- **On Chip Voltage Multiplier Provides 4.5V For Driving 3½ Digit Field Effect Display**
- **Only Two Switches Required For Complete Operation Of The Watch**
- **Operates With 32.768 kHz Quartz Crystal**
- **Anti-Bounce Protection On Switch Inputs**
- **AM/PM Indication When Setting Time**

The 5810A is a low power timekeeping circuit intended for use with 7 segment, 3-1/2 digit field effect liquid crystal displays. All of the circuitry required in a Time/Seconds/Date watch is contained on this single chip.

An on-chip voltage multiplier is incorporated on the 5810A. The multiplier derives a 4 to 4.8 volt display drive supply from the 1.5 volt battery. This multiplier requires only three external capacitors.

The 5810A, in conjunction with an external quartz crystal and trimmer capacitor, oscillates at 32.768 kHz, divides down and decodes Seconds, Minutes, Hours, and Date of Month.

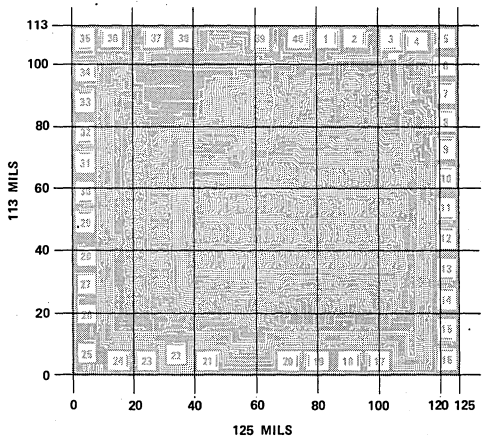
The 5810A will normally display Hours and Minutes. Closure of the D/C command switch will cause Seconds to be displayed in the Minutes position and the Hours will be blanked. A second closure of the D/C command switch will cause the Date to be displayed in the Minutes position and Hours to be blanked. A third closure of the D/C command switch will cause a return to the normal mode displaying Hours and Minutes. Switch S is used in conjunction with switch D/C for timesetting operations (see page 11-4 for description of operation). Thus only two switches are required for complete operation of the watch.

The colon is flashed at a 1Hz rate in all three display modes.

To facilitate testing and calibration a fast test input, reset and oscillator calibrate output are provided. These functions are described on page 11-4.

The 5810A is manufactured with complementary silicon gate MOS. This extremely low power technology is ideally suited for the manufacture of devices designed to operate on small batteries for long periods of time.

CHIP TOPOGRAPHY



PAD ASSIGNMENT

1. D/C	21. B3
2. S	22. Fast Test
3. VDD	23. C3
4. GND	24. D3
5. Cap 1	25. E3
6. Cap 1	26. C2
7. Cap 2	27. A2 + D2
8. Cap 2	28. E2
9. VTT	29. L
10. G1	30. C1
11. F1	31. D1
12. A1	32. E1
13. B1	33. K
14. G2	34. Common
15. F2	35. Calibrate Out
16. A2 + D2	36. Oscillator Cap 1
17. B2	37. Oscillator Cap 2
18. G3	38. Oscillator Out
19. F3	39. Oscillator In
20. A3	40. Reset

Absolute Maximum Ratings*

Temperature Under Bias ..... −20°C to +70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage V_{DD} with respect to GND ..... -8.0V to +0.3V
Voltage on all Inputs or Outputs with respect to GND ..... V_{DD} -0.3V to +0.3V
Power Dissipation 100mW

COMMENT:

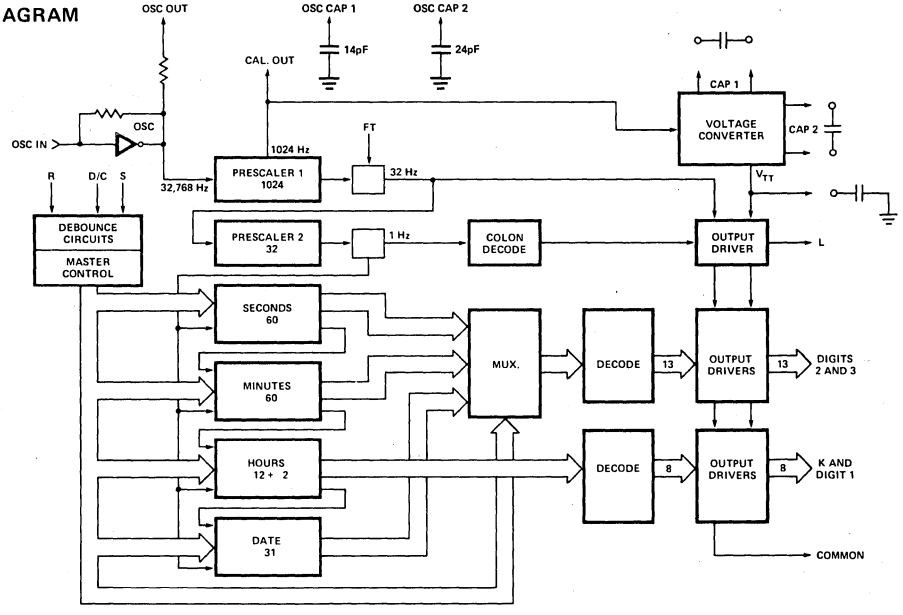
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

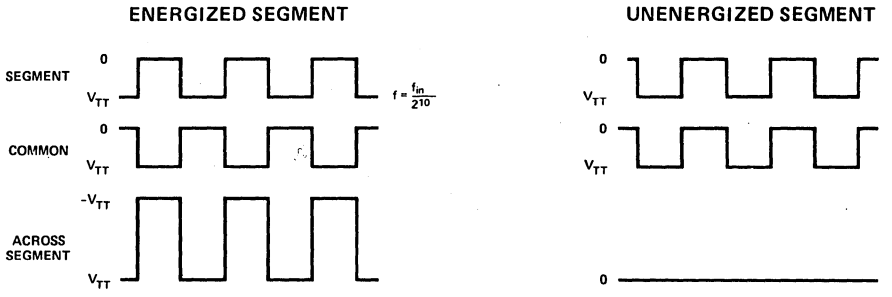
T_A = 25°C; V_{DD} = -1.6V; f_{OSC} = 32.768 kHz, Unless Otherwise Specified.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
I_{DD}	Total Average Internal Current		5	μA	No Output Load
			10	μA	1μA Output Load
V_{TT}	Multiplier Output Voltage		-4.8	V	I_{OUT} = 0.0μA
		-4.0		V	V_{DD} = 1.5V, I_{OUT} = 1.0μA
I_{IHS}	Switch Input High Current (D/C, S)		4	μA	V_{IN} = 0V
V_{IL}	Input Low Voltage	V_{DD}-0.3	V_{DD}+0.4	V	
V_{IH}	Input High Voltage	-0.3	0.3	V	
V_{DD} START	Minimum Oscillator Start Voltage	-1.4		V	
V_{DD} SUST	Minimum Oscillator Sustaining Voltage	-1.3		V	
V_{OLC}	Output Low Voltage Common		V_{TT}+0.1	V	V_{TT}=-4.0V; I_{OLC}=1.0μA
V_{OHC}	Output High Voltage Common	-0.1V		V	V_{TT}=-4.0V; I_{OHC}=-1.0μA
V_{OLS}	Output Low Voltage Segment		V_{TT}+0.1	V	V_{TT}=-4.0V; I_{OLS}=50nA
V_{OHS}	Output High Voltage Segment	-0.1V		V	V_{TT}=-4.0V; I_{OHS}=-50nA

BLOCK DIAGRAM

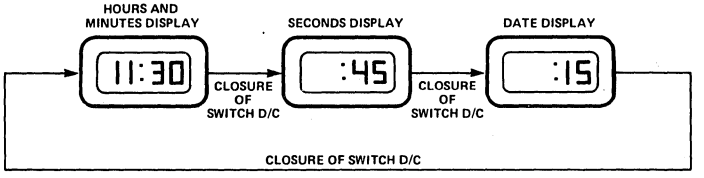


Output Waveforms



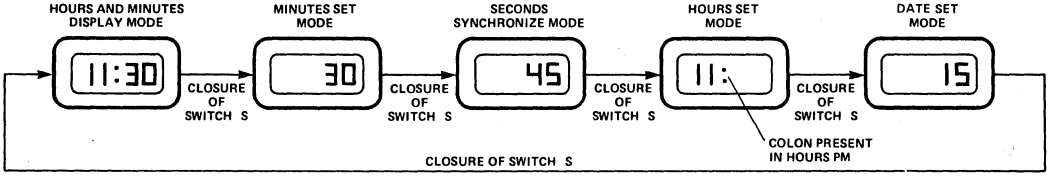
Time Display

Switch input D/C controls the time display modes. Each closure of switch D/C (D/C input = high) causes a change in the display mode in the sequence Hours and Minutes→Seconds→Date→Hours and Minutes. The following diagram illustrates this:



Time Setting

Switch input S controls the time setting modes. This switch input is active only when the circuit is in the Hours and Minutes display mode. Each closure of switch S (S input = high) causes a change in the time set modes in the sequence Hours and Minutes→Minutes→Seconds →Hours→Date→Hours and Minutes. *Closure of switch D/C when in the Minutes, Hours, or Date time set modes will cause that mode to be advanced at a 1 Hz rate. Closure of switch D/C in the Seconds synchronize mode will cause the Minutes to be advanced by one and the Seconds to be reset to zero and held until the D/C input is returned high.* The colon is displayed only in the Hours PM state in the time set mode. The following diagram illustrates this:



Reset

The reset input may be used to initialize all time counters to the zero state. All time counters are automatically reset to zero when voltage is initially applied to the circuit. The zero state is 12:00 AM, 00 Seconds, 0 Date.

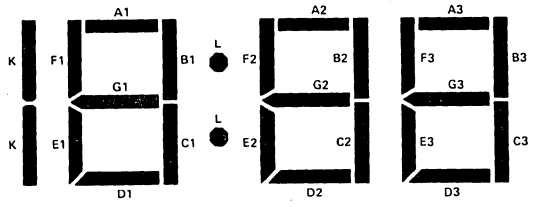
Fast Test

This input by-passes the oscillator stage and prescaler 1, allowing cycling of the counters at rates faster than real time.

Calibration Output

This output brings out the oscillator frequency divided by 32 and may be used for calibration of the oscillator.

Display Segment Format



DIGITS D1, D2 AND D3 TRUTH TABLE

NUMBER	SEGMENTS						
	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Typical Application